Remarks

Information Disclosure Statement.

The Examiner is requested to return a copy of the Form 1449/PTO which was submitted in a Supplemental Information Disclosure Statement (with the required fee), in Applicant's response filed June 6, 2003. A copy of this submission is enclosed herewith.

Also enclosed is a Supplemental Information Disclosure Statement and Form 1449/PTO listing references for consideration. Since this IDS is being filed as part of the RCE, no fee is due for consideration of the listed items.

Consideration of the listed references is requested, and return of the enclosed Form 1449/PTO (*and* previously filed Form 1449/PTO) is requested showing the references as being initialed and considered.

Rejection of the claims.

Reconsideration of pending Claims 101-116 and 123-223 is respectfully requested.

Item 5(1) of the Advisory Action.

In the Advisory Action, the Examiner responded to Applicant's responsive arguments by maintaining the rejection of the claims based on **Miyano**, **Ishida**, **Moslehi**, and **Saihara**.

The Examiner maintains the rejection of the claims based on the primary references of Miyano and Moslehi for the following reasons:

a) Epitaxial is a process, thus it would not lend patentability to the product.

b) Two overlying epitaxial silicon layers would not be distinguishable over a single, double or multiple epitaxial silicon layer in the final structure.

c) Moslehi discloses that two epitaxial silicon layers can be combined into one layer, at col. 20, lines 12-19, to create a final structure in FIG. 19.

Applicant believes that the Final Rejection is in error because:

1) The Examiner has mischaracterized the phrase "epitaxial silicon layer."

2) The Examiner's assertion that overlying epitaxial silicon in Applicant's structures can not be distinguished is in error.

3) The formation of a single epitaxial layer by Moslehi does not obviate Applicant's structures as claimed.

4) Miyano does not anticipate Applicant's structures as claimed.

5) The combination of Miyano with Ishida will not result in Applicant's structures as claimed.

6) Ishida teaches away from Applicant's structure.

7) The combination of Moslehi with Wu would not result in Applicant's structures as claimed.

8) There is no motivation to modify Moslehi's structure based on Wu.

9) The combination of Moslehi with Saihara does not obviate Applicant's structures as claimed.

10) Saihara teaches away from an epitaxial layer having a faceted surface.

1) The Examiner has mischaracterized the term "epitaxial silicon layer."

At paragraph 1(a) of the Advisory Action, the Examiner asserted that the feature of two or more overlying layers of "epitaxial silicon" in the claims does not lend patentability to the claimed structures.[1] The Examiner has evidently mischaracterized the term "epitaxial silicon" as that term is understood in the art — including other U.S. patents.

The use of the term "epitaxial silicon" in the context of the claim is not a process limitation.

The term "epitaxial" in the context of the claims is used *as an adjective* to describe the structure of the silicon layers. The term "epitaxial silicon" is an art-based term meaning a *single crystal silicon film/layer.*

[1] It is noted that in Applicant's response (mailed February 20, 2003), the claims were previously amended to replace the phrase "epitaxially grown silicon" with the phrase "epitaxial silicon" in order to eliminate a *purported* process limitation from the claims. The amendments were made in response to the Examiner's statements that "...the process limitations "epitaxially grown silicon" in claim 101 [129] do not carry weight in a claim drawn to structure..." citing to *In re Thorpe*, 277 USPQ 964 (Fed. Cir. 1985). See Office Action mailed November 27, 2002, at pages 6 and 10.

The Examiner is respectfully directed to the following definitions of the term "epitaxial":[2]

1) Van Zant, Peter, *Microchip Fabrication*, 4th ed., page 602, McGraw-Hill, NY, NY (2000) — which defines the term "epitaxial" as follows:

> **epitaxial**....The growth of a single-crystal semiconductor film upon a single crystal substrate...

2) *Webster's New World Dictionary*, 3rd ed., page 458, V. Neufeldt (ed.), Simon & Schuster, Inc., NY, NY (1988) — **which notes "epitaxial" as an *adjective***:

> **epitaxy**...***n***....the overgrowth in layers of a crystalline substance deposited in a definite orientation on a base or substratum composed of different crystals — **ep'|i tax'I|al or ep'|i tax'|ic** ***adj.***

Claims of other U.S. patents further demonstrates the accepted meaning and use of "epitaxial silicon layer" to characterize semiconductor *structures and devices*. For example, the Examiner is directed to the following patents and claims (copy enclosed)

USP 6,410,370 (Grass)

> 14. A semiconductor device comprising: **an epitaxial silicon layer** over said first and second metal layers.

USP 5,753,947 (Gonzalez)

> 1. A semiconductor structure comprising: ...(c) **a silicon epitaxial layer** formed on said plurality of digit lines, said epitaxial layer being referred to as a word line and comprising:

USP 5,600,161 (Gonzalez)

> 2. The active transistor of claim 1, wherein said semiconductive region comprises **selective epitaxial grown (SEG) silicon**.

USP 5,973,396 (Farnworth)

> 3. A semiconductor die structure, comprising: ...**an epitaxial layer** extending over at least a portion of the front side of the semiconductor die substrate and the at least one electrically conductive via...

The term "epitaxial" in the context of the present claims defines the *character* and *structure* of the silicon layers of Applicant's claimed structures. The Examiner's statement that the term "epitaxial silicon" in the claims is a process limitation and does not lend patentability to the claimed structures is clearly in error.

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[2] The Examiner is also directed to Applicant's response (mailed February 20, 2003) and the discussion of epitaxial silicon at pages 6-7.

2) The Examiner's assertion that overlying epitaxial silicon in Applicant's structures can not be distinguished is in error.

At paragraph 1(b) of the Advisory Action, the Examiner apparently questions the ability to distinguish two overlying epitaxial silicon layers from a single epitaxial silicon layer in the final structure.[3]

The Examiner is respectfully directed to Applicant's response (mailed February 20, 2003) and the discussion of epitaxial silicon at pages 6-7.

An epitaxial silicon film has a single crystalline structure and can be distinguished by the presence of a faceted top surface. The structure of an epitaxial film on a substrate can be examined by cross-sectioning and, for example, by scanning electron microscope (SEM) or transmission electron microscope (TEM), as known and used in the art. (This is discussed in the specification at page 9, lines 16-19.)

The Examiner is also directed to the following published documents that discuss the use of scanning electron microscopy (SEM) and other techniques known in the art to view epitaxial layers in a multilayer structure:

USP 5,888,294 (Min et al.), e.g., at col. 2, lines 23 to col. 3, line 31, and the figures.

US 2001/0040292 (Hahn et al.) at paragraphs [0016] and [0032] and FIGS. 3A-3B.

Blanton and Hung, *X-ray diffraction characterization of multilayer epitaxial thin films deposited on (0001) sapphire*, The Rigaku Journal 13(1) (1996) (at page 3, col. 2):

> Knowledge of the microstructure of thin films....Several techniques are applied for this microstructure characterization including scanning electron microscopy (SEM), atomic force microscopy (AFM), Rutherford backscattering spectroscopy (RBS), secondary ion mass spectroscopy (SIMS), micro Raman spectroscopy (μRS), X-ray photoelectron spectroscopy (XPS), and X-ray diffraction (XRD)...

It is clear that one skilled in the art could readily be able to distinguish and differentiate two or more layers of epitaxial silicon in a semiconductor structure compared to a single epitaxial silicon layer, using techniques that are known and widely used in the art to characterize epitaxial thin film layers.

The Examiner statement that overlying epitaxial silicon layers cannot be distinguished from a single epitaxial silicon layer in the final structure is clearly without merit.

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[3] The claims recite "*at least two* overlying layers of epitaxial silicon." Claim 194 recites "*two or more* overlying layers of epitaxial silicon." (emphasis added) It is noted that "at least two overlying layers of epitaxial silicon" includes double or multiple epitaxial silicon layers.

3) The formation of a single epitaxial layer by Moslehi does not obviate Applicant's structures as claimed.

At paragraph 1(c) of the Advisory Action, the Examiner stated as follows:[4]

> "As evident in Moslehi reference, two epitaxial silicon layers can be combined into one layer, column 20 lines 12-19, to create a final structure in fig. 19."

The relevancy of the Examiner's point is not understood. Applicant is claiming structures made of *at least two overlying layers* of epitaxial silicon. This passage in Moslehi teaches forming a single epitaxial silicon layer — which essentially *teaches away* from Applicant's invention of a semiconductor structure having *two or more layers* of epitaxial silicon.

4) Miyano does not anticipate Applicant's structures as claimed.

The Examiner previously rejected Claims 101-102, 106-109, 194, and 196-223 under Section 102(e) as anticipated by **Miyano** (USP 6,232,641). The Examiner's only response to Applicant's responsive arguments to the rejections of the claims based on Miyano was in paragraph 5(1) of the Advisory Action.

Apparently, the Examiner maintains the rejection based on Miyano on the basis that (a) two or more overlying epitaxial silicon layers cannot be distinguished from a single epitaxial silicon layer, and (b) two epitaxial silicon layers can be combined into a single epitaxial silicon layer (referring to Moslehi).

As stated above with regard to Paragraph 1 of the Advisory Action, one of ordinary skill in the art would readily be able to distinguish and differentiate two or more overlying layers of epitaxial silicon compared to a single epitaxial silicon layer using known techniques.

Moreover, the formation of a single epitaxial silicon layer is not Applicant's invention *as claimed*.

The Examiner's rejection under §102(e) is in error because the Examiner has failed to apply the correct standards of anticipation. In order for the subject matter of a claim to be anticipated under 35 U.S.C. §102, the prior art reference must teach every aspect of the claimed invention either explicitly or implicitly. See MPEP §706.02. The Federal Circuit has

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[4] The Examiner misstates the passage in Moslehi at col. 20, lines 12-19, which correctly recites (emphasis added): "...If desired, *the two SSG processes can be combined into one SSG process* in order to reduce processing complexity..."

consistently upheld this "all elements" test for anticipation. *See, e.g., Hybritech Inc. v. Monoclonal Antibodies, Inc.*, 231 USPQ 81, 90 (Fed. Cir. 1981) ("it is axiomatic that for prior art to anticipate under §102 it has to meet every element of the claimed invention, and that such a determination is one of fact."); *In re Donohue,* 226 USPQ 619, 621 (Fed. Cir. 1985) ("an anticipation rejection requires a showing that each limitation of a claim must be found in a single reference, practice, or device."); *Atlas Powder Company v. E.I. du Pont De Nemours & Company,* 224 USPQ 409, 411 (Fed. Cir. 1984) ("exclusion of a claimed element from a prior art reference is enough to negate anticipation by that reference"). Likewise, the MPEP further elaborates the all elements anticipation test in §2131. Specifically, MPEP § 2131 states:

> A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference.' 'The identical invention must be shown in as complete detail as is contained in the . . . claim'.

Miyano does not disclose all the elements of the claims as required under Section 102(e). In particular, Miyano does not disclose *at least two overlying layers of epitaxial silicon* as claimed by Applicant.

Miyano teaches a *single* epitaxial layer **12** that is formed on the S/D regions in silicon substrate 1. This is illustrated in FIG. 6I and 6J below, and discussed at col. 10, lines 51-56:

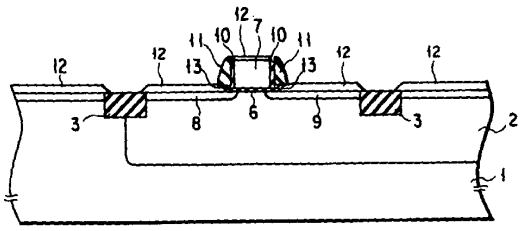

FIG. 6I

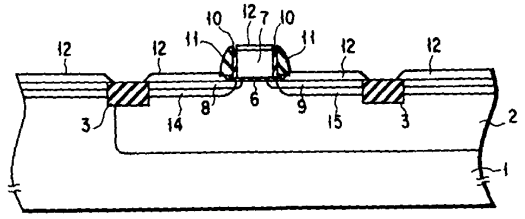

FIG. 6J

> Then, as shown in FIG. 6I, a vapor phase epitaxial growth method is employed to form an epitaxial silicon film (a single crystal silicon film) 12 having a thickness of about 50 nm on the source diffusion layer 8 and the drain diffusion layer 9 allowed to appear after the SiO_2 liner 10 and the gate oxide film 6 have been removed.

Miyano then teaches forming a ***metal silicide film 16*** over the epitaxial silicon film 12, and deposits an insulating film 17 *over the metal silicide film 16.* This is shown in FIG. 6K below, and discussed at col. 11, lines 41-54 (emphasis added):

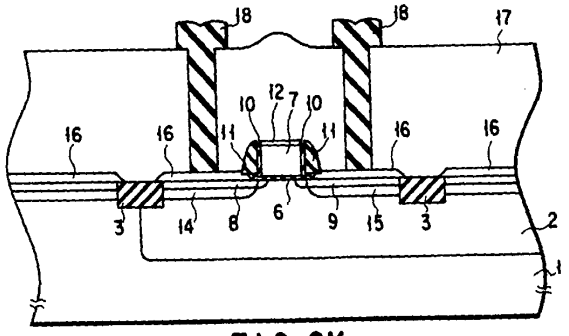

FIG. 6K

> Then, as shown in FIG. 6K, ***a usual silicide technique is employed to form a metal silicide film 16*** in a self-aligning manner, **and then an interlayer insulating film 17 is deposited on the overall surface.**
>
> ...
>
> In this embodiment, the overall body of ***the epitaxial silicon film 12 is formed into the silicide structure to form the metal silicide film 16***. Note that only the upper portion of the epitaxial silicon film 12 may be converted into the metal silicide film 16.

Miyano's structure — which is made of a single epitaxial silicon layer with a metal silicide layer over the top of the single epitaxial layer — does not anticipate Applicant's structure made of *at least two overlying layers of epitaxial silicon*, and an *insulative material layer* disposed over the top surface of the uppermost epitaxial layer. Accordingly, withdrawal of the § 102 rejection of the claims based on Miyano is respectfully requested.

5) The combination of Miyano with Ishida will not result in Applicant's structures as claimed.

The Examiner rejected Claims 103-104 and 110 as obvious over **Miyano** in view of **Ishida** (USP 6,051,473). The Examiner rejected the claims on the basis that it would be obvious to combine the S/D regions of Ishida (two overlying layers of epitaxial silicon 250, 260) into the structure of Miyano.

This combination would not produce Applicant's structures as claimed.

The Examiner is referring to Ishida's description of prior art raised S/D structures, such as the S/D structure shown in (prior art) FIG. 2 below, which includes epitaxial layers 250, 260:[5]

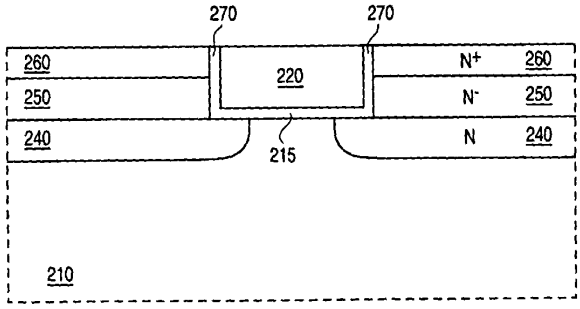

FIG. 2
(PRIOR ART)

Ishida includes a similar structure shown in (prior art) FIG. 3F below, which includes epitaxial layers 350, 360:[6]

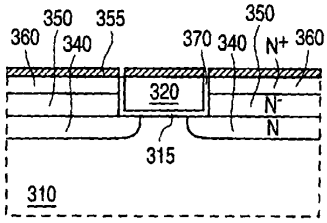

FIG. 3F
(PRIOR ART)

As shown in FIG. 3F — the uppermost S/D layer 360 is *silicided* — that is, the epitaxial silicon layer is reacted with a metal to form a ***metal silicide layer 355***. See Ishida at col. 2, lines 47-57 (emphasis added):

> Finally in FIG. 3F, the raised source-drain regions 360 and gate region 320 is **silicided**--that is, a conductive material such as titanium is applied followed by heat cycles **causing the conductive material to react with the silicon** (but not the oxide) **and form, for instance, $TiSi_2$ 355**. Other silicide compounds may also be satisfactory. Typically, in conventional MOSFETs, **as the silicide forms, it eats into and reduces the source and drain regions**. . .

[5] See description in Ishida at cols. 1-2.

[6] See description in Ishida at col. 4, lines 14-63.

Ishida does not teach or suggest an insulative material layer disposed over the top surface of the uppermost epitaxial layer as required by Applicant's claims. Rather, Ishida — *like Miyano* — teaches the formation of a metal silicide layer (355) on the surface of the exposed surface of the uppermost silicon layer (360).

Nor does Ishida teach each of the epitaxial layers having insulated sidewalls. Ishida merely teaches sidewall oxide 270 (prior art FIG. 2) and 370 (prior art FIG. 3) that are formed *adjacent to the gate* prior to formation of the S/D regions 340 *and* the epitaxial layers 350, 360 —to protect and isolate the gate from the S/D regions (at col. 4, lines 23-28; emphasis added):

> After the gate structure is formed, sidewall oxides 370 are formed by growing or depositing an oxide surrounding gate 320 ***to isolate the gate*** from the raised source and drain regions as shown in FIG. 3B....
> *Once the gate has been adequately protected*, source and drain regions 340 are formed...

Referring again to (prior art) FIG. 2, Ishida reiterates that the purpose of the sidewall oxides 270 is to control capacitance between the gate and the raised S/D regions 250, 260, and that the sidewall oxides 270 are formed on the gate *prior to* forming epi layers 250, 260 (at col. 2, lines 48-57, emphasis added):

> Finally, the quality of the sidewall oxides 270 in these raised source-drain MOSFETs is generally lacking. Sidewalls of sufficient uniform thickness are necessary to control capacitance between the gate and the raised source-drain regions 250 and 260. Such sidewall oxides however, are ***generally grown or deposited on the gate prior to forming epi layers 250 and 260***, and the ability to form sidewalls of adequate uniform thickness to sufficiently control capacitance is extremely difficult, particularly when subjected to the cycles required for epitaxy.

Thus, Ishida does not teach or suggest the formation of sidewall oxide spacers on the sidewalls of each of the epitaxial layers 250, 260 (or 350, 360) — only the oxide spacers 370 on the sidewalls of the gate region 320.

The Examiner has failed to establish a *prima facie* case of obviousness rejection of the claims based on a combination of Miyano with Ishida. Both Miyano and Ishida teach depositing a refractory metal layer over an uppermost epitaxial silicon layer of a structure, and reacting the metal layer with the underlying silicon layer to form a refractory metal silicide contact. Neither reference teaches or suggests Applicant's structures as claimed having at least two overlying epitaxial silicon layers *and an insulative material layer* disposed on the top surface of the uppermost epitaxial layer, *and insulative spacers* on the sidewalls of each epitaxial silicon layer.

6) Ishida teaches away from Applicant's structure.

It is further submitted that Ishida expressly *teaches away* from the fabrication of a S/D made of raised epitaxial layers. A reference teaches away when "a person of ordinary skill, upon reading the reference ... would be led in a direction divergent from the path that was taken by the applicant." *In re Gurley*, 313 USPQ2d 1130, 1131 (Fed. Cir. 1994).

In particular, Ishida is directed to solving problems with raised S/D regions that have been conventionally formed by epitaxial growth processes. Ishida's solution is to form raised S/D regions by depositing a layer of doped amorphous silicon on a substrate.

In discussing prior art S/D structures, Ishida emphasized the problems of fabricating epitaxially grown S/D regions (See above at prior art FIG. 2, and discussion in Ishida at col. 2, lines 29-61, emphasis added):

> ...use of raised source-drain MOSFETs has not become widespread. **The devices are difficult to manufacture for at least three reasons. First**, as shown in the HCS device of FIG. 2, *the raised epitaxial layers 250 and 260 must be selectively grown, which is a difficult task* involving high vacuum and chemical vapor deposition processes. Such processes further require expensive equipment, are difficult to control, critically rely on surface preparation, and are easily ruined by a small amount of contamination.
>
> **Second**, source and drain regions 240 are doped using conventional methods, e.g., by ion implantation, prior to forming the epitaxial layers...*the heat cycles in the epitaxial (epi) layer formation cause the dopants to diffuse.*
>
> **Finally**, the quality of the sidewall oxides 270 in these raised source-drain MOSFETs is generally lacking. Sidewalls of sufficient uniform thickness are necessary to control capacitance between the gate and the raised source-drain regions 250 and 260. Such sidewall oxides however, are generally grown or deposited on the gate prior to forming epi layers 250 and 260, and *the ability to form sidewalls of adequate uniform thickness to sufficiently control capacitance is extremely difficult, particularly when subjected to the cycles required for epitaxy.*
>
> Therefore, it is desirable to develop a process that will allow for easier manufacturability of raised source-drain MOSFETs, and thus allow for semiconductor device formation of reduced size.

Ishida again addresses the problems with forming epitaxial S/D structures in a discussion of the prior art structures shown in FIGS. 3A-3F (see above at prior art FIG. 3F, and discussion at col. 4, lines 34-39 and 58-63, emphasis added):

> Next, an N^- region 350 is selectively epitaxially grown on silicon substrate 310 over the source and drain regions 340... **Epitaxial growth is a highly complicated process which is extremely difficult to control**...
>
> .....
>
> **Because selective epitaxial growth of layers 350 and 360 is difficult, and** because the various heat steps, including those occurring during epi growth and silicide formation, cause diffusion of source and drain regions 340, the method described with reference to FIGS. 3A-3F **is considered impractical.**

Thus, Ishida may fairly be said to *teach away* from the current invention of forming an S/D structure of overlying epitaxial silicon layers.

Clearly, based on the explicit teaching of Ishida *against* the formation of S/D regions of epitaxial silicon layers, there is no motivation to modify Miyano's structure to incorporate S/D regions made of epitaxial silicon layers. The Examiner's rejection of the claims based on the proposed modification of Miyano with Ishida is clearly without merit and should be withdrawn.

Accordingly, based on the above remarks, withdrawal of the rejection of the claims based on the combination of Miyano with Ishida is respectfully requested.

7) The combination of Moslehi with Wu would not result in Applicant's structures as claimed.

The Examiner rejected Claims 101-116, 123-130, 132-135, 137-160 and 165-223 under Section 103(a) as obvious over **Moslehi** in view of **Wu** (USP 5,902,125). The Examiner rebutted Applicant's previously submitted arguments, stating as follows (emphasis added):

> The Applicant also argues that the deposit of an oxide layer that would isolate the semiconductor layer 92 and 94 of Moslehi's structure would be contrary to Moslehi's process for forming metal interconnect segment 98 and 100. This is not persuasive **because the** ***interconnect 98 and 100 would provide a good source, drain and gate contact structures***, such structure is similar to that of Wu's fig. 7, contacts 18 and 20. **Furthermore,** ***an oxide layer or inter dielectric layer can be deposited on the entire structure including interconnect segment 98 and 100***. The purpose of such dielectric layer is providing the structure isolation or protection and for further processing such as plug contact, which is common in the art, as is described by Wu in fig. 8. Therefore, the deposit of an oxide layer would not isolate the structure, but it rather provides the structure protection.

Applicant does not dispute the Examiner's statement that interconnect 98 and 100 shown in FIG. 19 of Moslehi would provide good contact structures to the source/drain junction regions 87 and the primary gate region 88. Nor does Applicant dispute the Examiner's statement that an oxide layer or inter-dielectric layer can be deposited on the entire structure of Moslehi including interconnect segments 98 and 100.

However, this structure does *not* obviate Applicant's semiconductor structures as claimed.

Applicant is claiming a structure that requires at least two overlying epitaxial silicon layers whereby an insulative material layer disposed over the top surface (and sidewalls) of the uppermost epitaxial layer, as illustrated in the following claims:

Claim 123: ...the uppermost epitaxial layer having *a top surface with an overlying layer of an insulative material...*

Claim 129: ...the uppermost epitaxial layer having *an insulated top surface...*

Claim 203: ...selectively growing a second epitaxial silicon layer ...comprising ... a top surface; and *depositing an insulative material layer thereover.*

Claim 204: ...and the uppermost epitaxial silicon layer comprises *an insulative film disposed on the top surface*...upon selectively growing the uppermost epitaxial silicon layer, depositing an insulative film layer thereover, with no subsequent removal of the insulative film layer from the top surface of said uppermost epitaxial silicon layer.

Moslehi does not teach or suggest a structure having at least two overlying epitaxial silicon layers and an insulative material layer disposed on the top surface (and sidewalls) of the uppermost epitaxial layer.

Moslehi specifically teaches (a) *depositing a refractory metal layer* onto the semiconductor (i.e., silicon) layer of the gate and S/D regions, and (b) performing an anneal ***to react the refractory metal layer with the underlying silicon layer*** — thereby *consuming* at least a portion of the underlying silicon layer — to form the refractory metal silicide contacts. Moslehi at col. 19, lines 24-56, and col. 20, lines 60-66 (emphasis added):

> FIG. 19 illustrates a cross-sectional view of transistor structure 36 of FIG. 18 following the formation of reacted refractory metal interconnect segments 98 and 100...Reacted refractory metal interconnect segments 98 and 100 are preferably formed in a three-step process. An RTA or furnace anneal is performed in order to form reacted refractory metal ***where the refractory metal reacts with a semiconductor substance in contact therewith***. It should be noted that FIG. 19 illustrates ***a complete reaction and consumption of the refractory metal with semiconductor segments*** 96, secondary elevated source/drain junction regions 92 and secondary upper gate region 94 (see FIG. 18). This complete consumption, however, is not necessary, but is merely shown for illustrative purposes.
>
> ...
>
> ...Additionally, the novel interconnect scheme provided in accordance with the present invention permits the formation of local interconnects ***utilizing reacted refractory metals with semiconductor underlayers*** and therefore eliminates the need for using refractory metal nitrides or high electrical resistance interconnects.

In contrast, the present invention requires an *insulative* material layer disposed on the top surface and sidewalls of the uppermost epitaxial layer of the source/drain junction regions and/or the gate region.

8) There is no motivation to modify Moslehi's structure based on Wu.

Applicant previously argued that the deposit of an oxide layer onto semiconductor layers 92, 94 of Moslehi's structure would be contrary to Moslehi's process for forming metal interconnect segments 98, 100.

The Examiner responded that Applicant's argument is not persuasive because "*an oxide layer or inter dielectric layer can be deposited on the entire structure including interconnect segment 98 and 100.*"

The Examiner apparently asserts that Applicant's structure is made obvious by the combination of Moslehi with the disclosure in Wu to deposit an oxide layer over the entire structure of Moslehi including the interconnect segments 98, 100.

The Examiner's reasoning fails because the *deposit of an oxide layer* over Moslehi's structure (shown in FIG. 19) would *not* result in Applicant's structure as claimed.

More specifically, to arrive at Applicant's structures as claimed would require a *modification* of Moslehi to deposit an *insulating layer* — rather than a ***refractory metal layer*** — onto the top surface of the silicon layers of the semiconductor segments 96, secondary elevated source/drain junction regions 92 and secondary upper gate region 94.

That modification would be inappropriate because it would be incompatible with the express teachings of Moslehi.

Where a proposed modification of a reference would destroy the intent, purpose or function of the disclosed subject matter, such a proposed modification is not proper, and a *prima facie* case of obviousness cannot be properly made. *In re Gordon*, 733 F.2d 900, 221 U.S.P.Q. 1124 (Fed. Cir. 1984).

As stated above, Moslehi specifically teaches in the context of the prior art of forming metal contacts to a transistor gate and source/drain regions. Moslehi is trying to solve the problem of the formation of refractory metal silicide contacts and the excess segments 35 in prior art structures (shown in FIG. 1) which are either removed or formed into less desirable TiN or Ti interconnects.

Moslehi's solution is to form a silicon layer over the S/D regions 92, the gate region 94, and the adjacent field isolation regions 42 — and then deposit a refractory metal layer 97 onto the exposed silicon layers, as shown in FIG. 18 below.

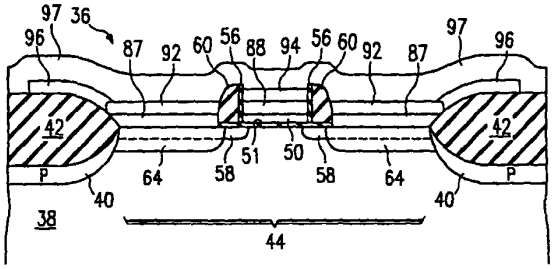

FIG. 18

Moslehi then performs an anneal to react the refractory metal layer 97 with the underlying silicon layers 92, 94 — shown below in FIG. 19 as being *completely consumed.* The result is the formation of refractory metal contacts 98, 100 (which replace silicon layers 92, 94, 96, and metal layer 97) — which are in contact with the silicon layers of the S/D and gate regions 87, 88.

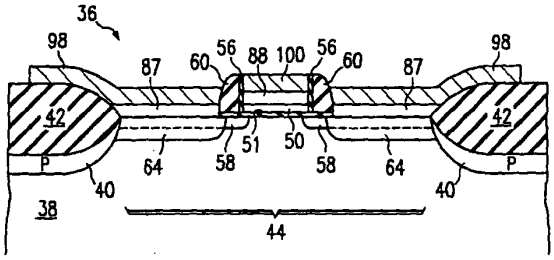

FIG. 19

The Examiner is selectively omitting a key part of the disclosed teaching of Moslehi, namely, *the deposit of a refractory metal layer onto the exposed surfaces of the silicon layers of the transistor S/D and gate regions to form refractory metal silicide contacts* over the top surface of the uppermost silicon layer.

Applicant's structures as claimed has *an insulation layer* disposed on the top surface (and sidewalls) of the uppermost silicon layer, which is clearly divergent from the structures taught by Moslehi. Thus, Moslehi may fairly be said to teach away from the current invention.

As for the disclosure of Wu, *like Moslehi* — Wu also teaches depositing and reacting a refractory metal layer with the epitaxial silicon layer 16 — to form a metal silicide layer 18 on the epitaxial silicon layer 16. As depicted below in FIG. 6, and discussed at col. 4, lines 55-59, Wu describes forming a single epitaxial silicon layer 16. (Note: epitaxial silicon layer 16[7] is ***exposed***.

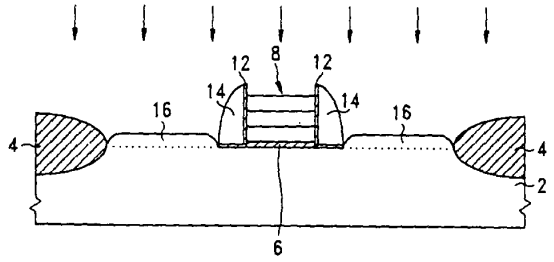

FIG.5

> Referring to FIG. 5, the ARC layer 10 is then removed to expose the top of the SAS layer 8. Then, a blanket ion implantation is carried out to implant p type dopant, such as boron or BF2 into the SAS layer 8, the epitaxial silicon 16 and silicon substrate 2 that under the epitaxial silicon 16...

Wu then teaches sputter depositing a refractory metal layer over the exposed epitaxial silicon layer 16 and the uppermost SAS layer 8 of the gate region, and *reacting the refractory metal layer with the epitaxial silicon layer 16* — to form a ***metal silicide layer 18*** on the epitaxial silicon layer 16. This structure is depicted in FIG. 6 below and discussed at cols. 4-5, bridging paragraph (emphasis added):

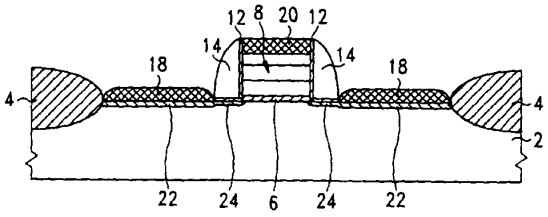

FIG.6

> ...As shown in FIG. 6, ***self-aligned silicide (SALICIDE) layer 18***, polycide layer 20 are respectively ***formed on the substrate 2 exposed by the gate structure***, and on the SAS layer 8. Typically, this can be achieved by using well known processes. For example, ***a refractory or noble metal layer***, such as Ti, Pt, Co, W, Ni etc, ***is sputtered on the substrate 2, gate structure. Then, a first-step rapid thermal annealing (RTA)*** at 350 to 700 centigrade degrees in N.sub.2 ambient ***is performed to react the refractory metal with*** the SAS layer 8 and ***the epitaxial silicon 16, thereby forming silicide on these portions...Therefore, the SALICIDE layer 18***,...

[7] Note that layer 16 is a single epitaxial silicon layer.

As noted, FIG. 6 shows the **metal silicide layer 18** has been formed *on the top surface and sidewalls* of epitaxial layer 16.[8]

In addition, *like Moslehi* — Wu also teaches depositing an oxide layer 26 onto the metal silicide layer 18 (and polycide layer 20). This is shown in FIG. 7 below, and discussed at cols. 4-5, bridging paragraph:

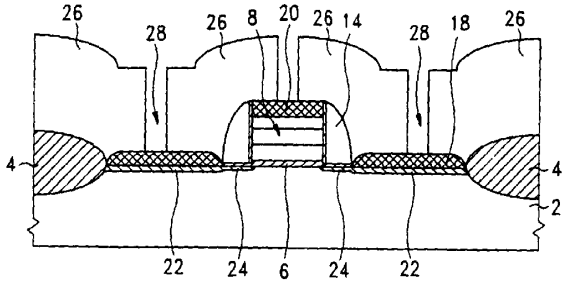

FIG.7

> Referring to FIG. 7, a thick oxide layer 26 is formed over the substrate 2 and gate structure for isolation...Then, contact holes 28 are generated in the oxide layer 26 and aligned to the source and drain 22 by using conventional manner.

Again, it is noted that the oxide layer 26 is formed onto the *metal silicide layer 18* — *not* the top surface and sidewalls of the *epitaxial layer 16* which is at least partly covered (and/or consumed) by the metal silicide layer 18.

It is also pointed out that Moslehi (like Wu) — in addressing prior art structures as depicted below in FIG. 1 — likewise describes forming an interlevel dielectric layer *over metal silicide contacts 98, 100* of the transistor 10.

[8] Layer 16 is shown in FIG. 5 above.

Moslehi describes (prior art) FIG.1 and the formation of a dielectric layer over the metal silicide contacts 32 at col. 9, line 39 to col. 10, line 3 (emphasis added):

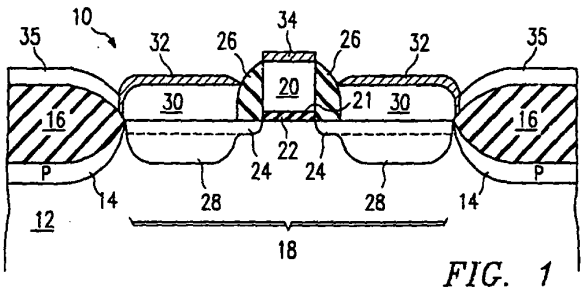

FIG. 1
(PRIOR ART)

> Additional considerations concerning elevated source/drain transistor 10 of FIG. 1 also arise with respect to excess segments 35. In particular, excess segments 35 are commonly formed simultaneously with the formation of **reacted refractory metal silicide contacts 32 and 34**. These regions are formed as a result of the sputter deposition of a thin refractory metal such as titanium or tungsten and a subsequent annealing step in a nitrogen or ammonia ambient. **The refractory metal titanium reacts with the semiconductor materials of elevated source/drain junction regions 30 and gate conductor 20, thereby forming electrically conductive reacted silicide regions for refractory metal silicide contacts 32 and 34, respectively**. Excess segments 35 are portions of either unreacted titanium or titanium nitride. These segments form over insulating layers due to the reaction between the deposited titanium and the nitrogen or ammonia ambient. This process is referred to as the self-aligned silicide or "SALICIDE" technique.
>
> The prior art has treated excess segments 35...In particular, after excess segments 35 (and sidewall ears) are removed, *an interlevel dielectric layer is formed over transistor 10 and contact holes are made within the dielectric layer. Thereafter, a metal layer is formed over the interlevel dielectric layer and metal contacts are made through the contact holes, thereby making connections to transistor 10...*

Both Moslehi and Wu teach (a) depositing a *refractory metal layer* over the surface (and sidewalls) of an uppermost epitaxial silicon layer of a structure, and *reacting* the metal layer with the underlying silicon layer to form a *refractory metal silicide contact*; and then (b) depositing an oxide layer onto the surface and sidewalls of the refractory metal silicide contact of the structure.

The Examiner has failed to establish a *prima facie* case of obviousness rejection of the claims based on the combination of Moslehi and Wu. Moslehi, either alone or combined with Wu, does not teach or suggest Applicant's structures as claimed having a) *at least two* overlying

epitaxial silicon layers, and b) *an insulative material layer disposed on the top surface (and sidewalls) of the uppermost epitaxial silicon layer.*

Accordingly, withdrawal of the rejection of the claims based on the combination of Moslehi with Wu is respectfully requested.

9) The combination of Moslehi with Saihara does not obviate Applicant's structures as claimed.

The Examiner rejected Claim 131 as obvious over **Moslehi** in view of **Saihara** (USP 5,963,822). Claim 131 depends from Claim 130 and ultimately from Claim 129.[9]

Claim 131 is directed to a structure comprising *at least two overlying layers* of epitaxial silicon — *each* silicon layer having a top surface defining a *facet* having a (100) plane orientation — and the uppermost epitaxial layer having an *insulated top surface.*

By comparison, Saihara describes methods for forming a *single* epitaxial film layer 3 on a surface of a (100) silicon substrate 1 — not at least two overlying epitaxial layers. This is illustrated for example, in FIG. 4C below.

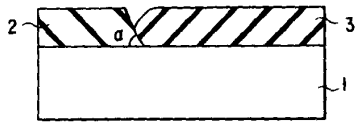

FIG. 4C

The Examiner rebutted Applicant's response, stating as follows:

> With respect to claim 131, the Applicant argues that Saihara describes single epitaxial silicon; see discussion of in the item 1 above.

The Examiner apparently maintains this rejection on the basis that: (a) at least two overlying layers of epitaxial silicon cannot be distinguished from a single epitaxial silicon layer

---

[9] Claim 129. A semiconductor structure, comprising: *at least two overlying layers of epitaxial silicon,* including an uppermost epitaxial layer; each epitaxial silicon layer comprising a top surface and insulated sidewalls, and the uppermost epitaxial layer having an insulated top surface; the structure disposed on a substrate in a vertical orientation.

Claim 130. The semiconductor structure of Claim 129, wherein *each epitaxial silicon layer comprises a top surface defining a facet.*

Claim 131. The semiconductor structure of Claim 130, wherein *the facet has a (100) plane orientation.*

in the final structure, and/or (b) two epitaxial silicon layers can be combined into one layer to create a final structure as shown in Moslehi's Fig. 19.

As stated above with regard to paragraph 1 of the Advisory Action, one of ordinary skill in the art would readily be able to distinguish and differentiate two or more overlying layers of epitaxial silicon compared to a single epitaxial silicon layer using known techniques.

Moreover, the formation of a single epitaxial silicon layer essentially *teaches away* from Applicant's invention of a semiconductor structure having two or more layers of epitaxial silicon.

Applicant's invention provides vertically stacked structures comprising *two or more* epitaxial silicon layers, such as transistor gates and elevated S/D regions. The vertical nature of the structures requires less surface area and provides for the fabrication of high density structures. In the formation of the claimed structures, Applicant employs insulative spaces formed on the sidewalls of each epitaxial layer to eliminate unwanted lateral growth and achieve vertically oriented structures formed of two or more epitaxial silicon layers.

The formation of a single epitaxial layer does not achieve Applicant's structures as claimed.

10) Saihara teaches away from an epitaxial layer having a faceted surface.

Furthermore, Saihara essentially *teaches away* from an epitaxial layer having a faceted surface. Saihara specifically teaches the fabrication of epitaxial films without a facet on the film surface. Saihara at col. 1, lines 5-10 (emphasis added):

> The present invention relates to a method of selectively forming an epitaxial film on a semiconductor substrate by using an insulating film as a mask and, more particularly, to a method of forming a selective epitaxial film ***which is improved not to form a facet*** on a selectively formed epitaxial film surface in contact with an insulating film.

This is emphasized by Saihara throughout the description, including the Summary at col. 2, lines 5-10 (emphasis added):

> The present invention has been made in consideration of the above situation, and has as its object to provide a method of forming a selective epitaxial film which can grow a selective epitaxial film having a flat growth surface **without any facet growth** by using no mask of an oxide film in a special shape such as a hangover shape.

To overcome the problem of facet growth on an epitaxial silicon layer, Saihara teaches annealing the selective epitaxial film layer to *eliminate* the facet from the surface of the layer. For example, see Saihara at col. 3, lines 51-63 (emphasis added):

> Silicon selective epitaxial growth at this time is performed...
>
> Subsequent to this selective epitaxial growth, annealing is performed...
>
> At this time, it was confirmed that the (111) facet 4 of the silicon selective epitaxial film 3 formed at the interface with the oxide film 2 was filled by the silicon selective epitaxial film 3 to eliminate the gap 25, as shown in FIG. 4C.

Thus, Saihara may fairly be said to teach away from the invention as recited in Claims 130-131.

Moreover, even if two overlying silicon epitaxial layers were formed — following Saihara teachings — each epitaxial silicon layer would not comprise a top surface defining a facet having a (100) plane orientation, as required in Claims 130-131, since Saihara anneals the epitaxial layers to *eliminate* the facet.

In addition, Saihara teaches a silicon epitaxial layer having a *(111) facet* — not a (100) facet as required in Claim 131. For example, see Saihara at col. 4, lines 21-23 (emphasis added):

> Accordingly, ***a (111) facet 4 is formed*** on the side surface of the p-type selective epitaxial film 23 on the oxide film 2 side, and a gap 25 is partially formed (FIG. 5B).

The Examiner has failed to establish a *prima facie* case of obviousness rejection of Claim 131. Moslehi, either alone or combined with Saihara, does not teach or suggest Applicant's structures as claimed having *at least two* overlying epitaxial silicon layers, *and* an *insulative material layer* disposed *on the top surface* (and sidewalls) of the uppermost epitaxial layer, with *each epitaxial silicon layer* having a top surface defining a *facet* having a *(100) plane orientation.*

Accordingly, withdrawal of the rejection of the claims based on the combination of Moslehi with Saihara is respectfully requested.

Extension of Term. The proceedings herein are for a patent application and the provisions of 37 CFR § 1.136 apply. Please consider this a petition for an extension of term and charge any fee required to Account No. 23-2053.

Based on the above remarks, the Examiner is respectfully requested to reconsider and withdraw the rejections of the claims. It is submitted that the present claims are in condition for allowance, and notification to that effect is respectfully requested.

Respectfully submitted,

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